IN THE CLAIMS:

Please cancel claim 1 without prejudice or disclaimer as indicated in the following.

Claims Listing:

1. – 11. (Canceled)

12. (Previously Presented) A system comprising:

a data processor having a first I/O buffer;

a memory having a second I/O buffer coupled to the first I/O buffer of the data processor,

the memory capable of storing code for:

establishing a set of encrypted links between a peripheral device and a software component, wherein establishing a first encrypted link of the set of encrypted links includes generating a first encryption key associated with a first port of encrypted data and establishing a second encrypted link of the set of encrypted links includes generating a second encryption key associated with a second port of encrypted data;

a hardware controller capable of outputting the first and the second encrypted links,

wherein the hardware controller includes:

a first register capable of storing information associated with the first encryption key;

a second register capable of storing information associated with the second encryption key;

a cipher component capable of :

receiving a single digital data stream;

applying the first encryption key to a first portion of the data stream; and

applying the second encryption key to a second portion of the data stream; and

a de-multiplexing component capable of splitting the single data stream into multiple data streams.

13. – 24. (Canceled)

25. (Previously Presented) A system comprising:

an interface capable of receiving a first and a second link of encrypted data from a hardware controller;

a first decryption component capable of decrypting the first link of encrypted data, using a first encryption key, to generate a first portion of a single received digital data stream;

a second decryption component capable of decrypting the second link of encrypted data using a second encryption key to generate a second portion of the received digital data stream; and

a multiplexing component capable of combining the first and the second portions of the received data streams to form a single received digital data stream.

26. (Original) The system as in Claim 25, further including:

a clock capable of clocking the single received data stream at twice the speed of the first and second links of encrypted data; and

a single processing component capable of processing the data associated with the first and the second links of encrypted data.